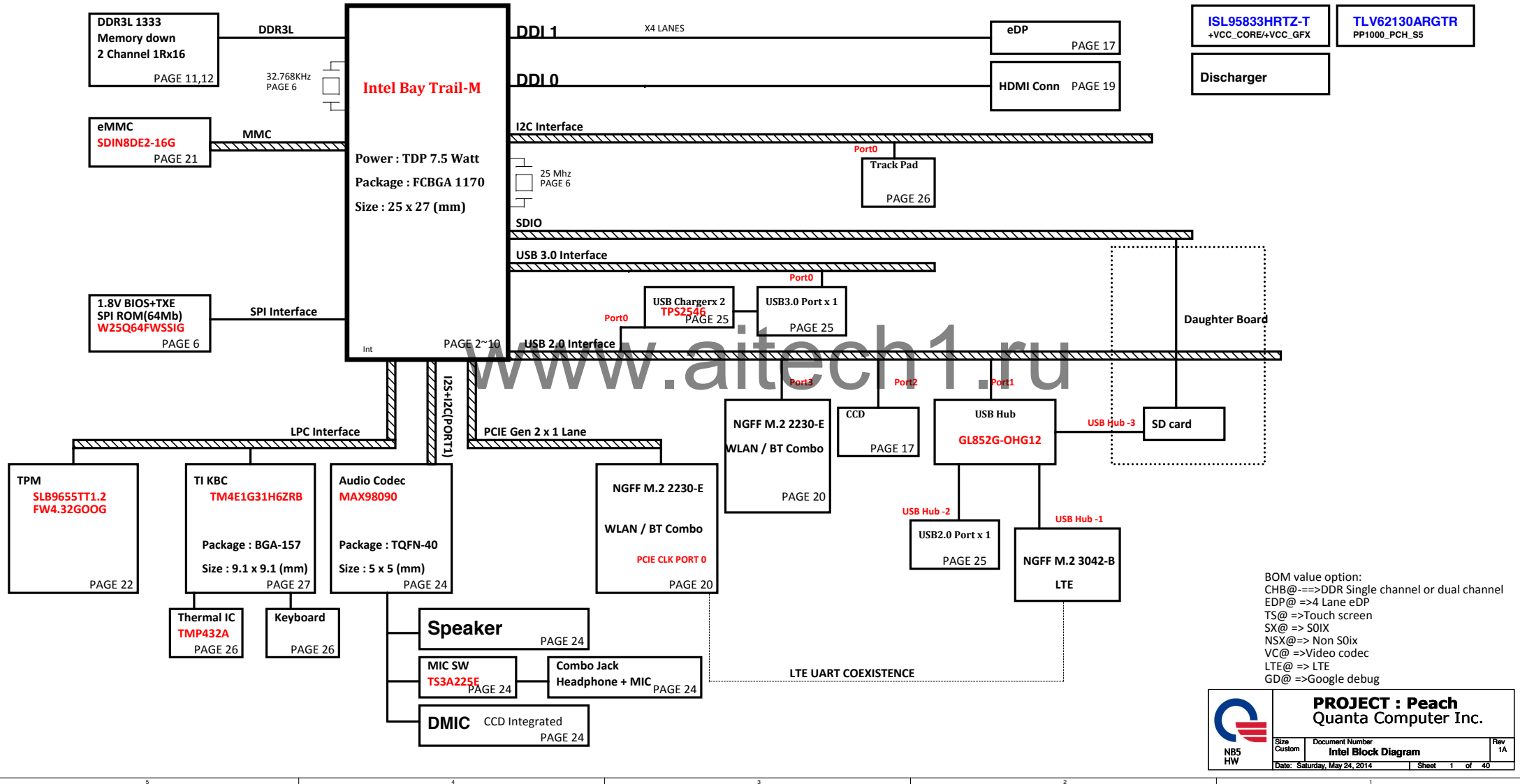
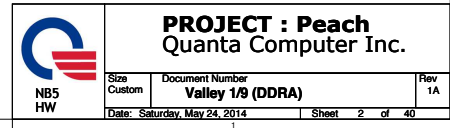


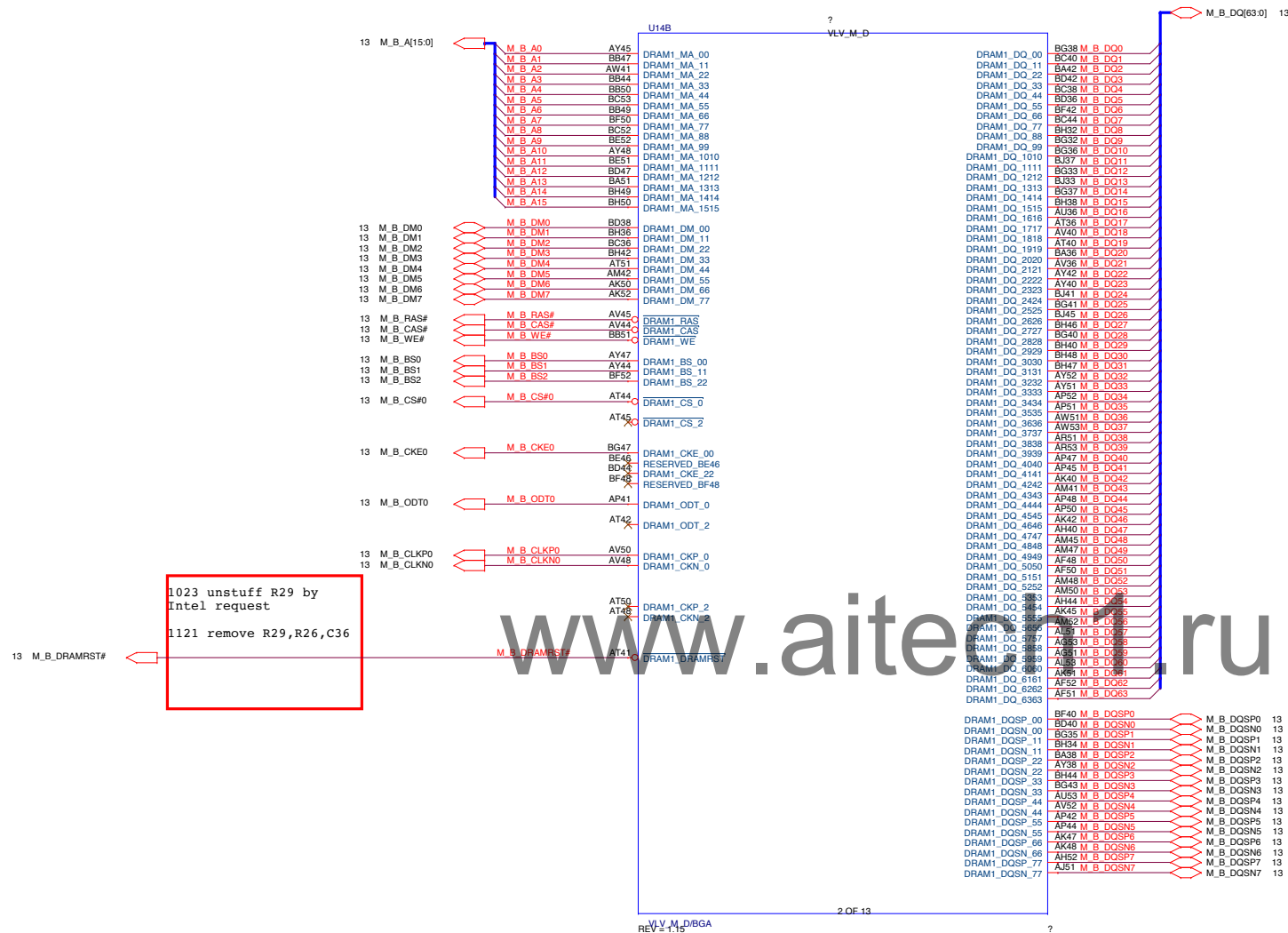
Intel Bay Trail-M Platform Block Diagram

SKUA QC N2920
AJ0QFW3UT05--CPU (1170P)N2920 1.86G QFW3(FCBGA)
SKUB DC N2820
AJ0QFW4UT02--CPU (1170P)N2820 2.13G QFW4(FCBGA)



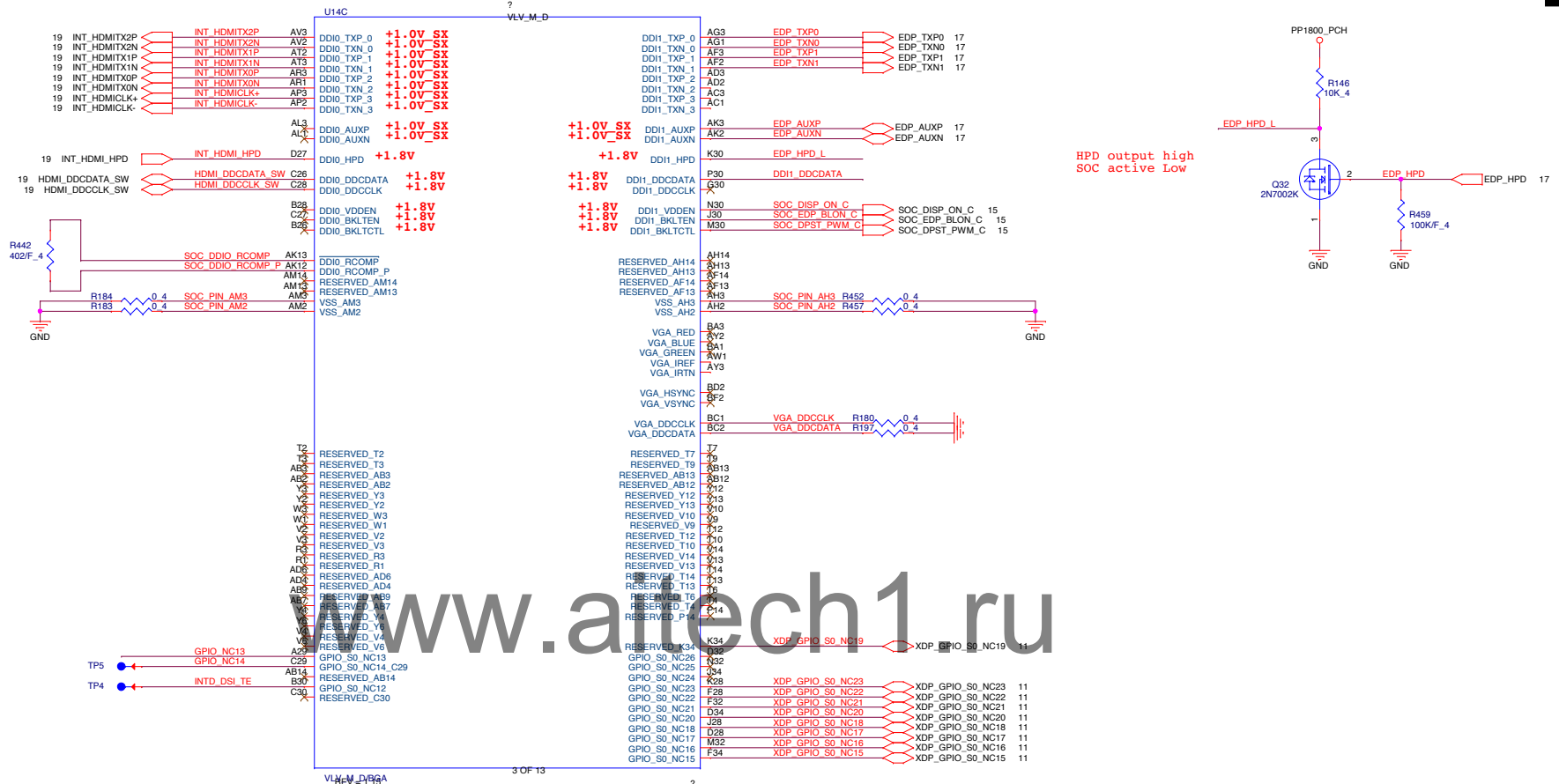


```
1023 unstuff R28 by
Intel request
1121 remove R28,R25,C35
```



PROJECT : Peach
Quanta Computer Inc.

Size Custom	Document Number Valley 2/9 (DDR8)	Rev 1A
Date: Saturday, May 24, 2014	Sheet 3 of 40	



BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	7 GPIO_SO_SC_56 PP1800_PCH R128 10K 4 R434 10K 4 GND
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	5 I2S_LRCLK PP1800_PCH R372 10K 4 R369 10K 4 GND
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	5 I2S_DOUT 27 SOC_OVERRIDE# R58 0.4 SOC_OVERRIDE NM 2 2N7002K GND
DDIO_DDCDATA	DDIO Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	HDMI DDCDATA SW R76 10K 4 GND
DDH1_DDCDATA	DDH1 Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	DDH1_DDCDATA R388 2.2K 4 R388 10K 4 GND
GPIO_SO_NC_13				GPIO_NC13 R62 10K 4 R63 10K 4 GND

1029 unstuff R128, using SoC internal PU

1029 unstuff R372, using SoC internal PU

1115 stuff R372, system can't boot if un-stuff R372 on proto1.5 board, need intel double confirm before proto2

1029 unstuff R386, using SoC internal PU

1115 stuff R386, it is required



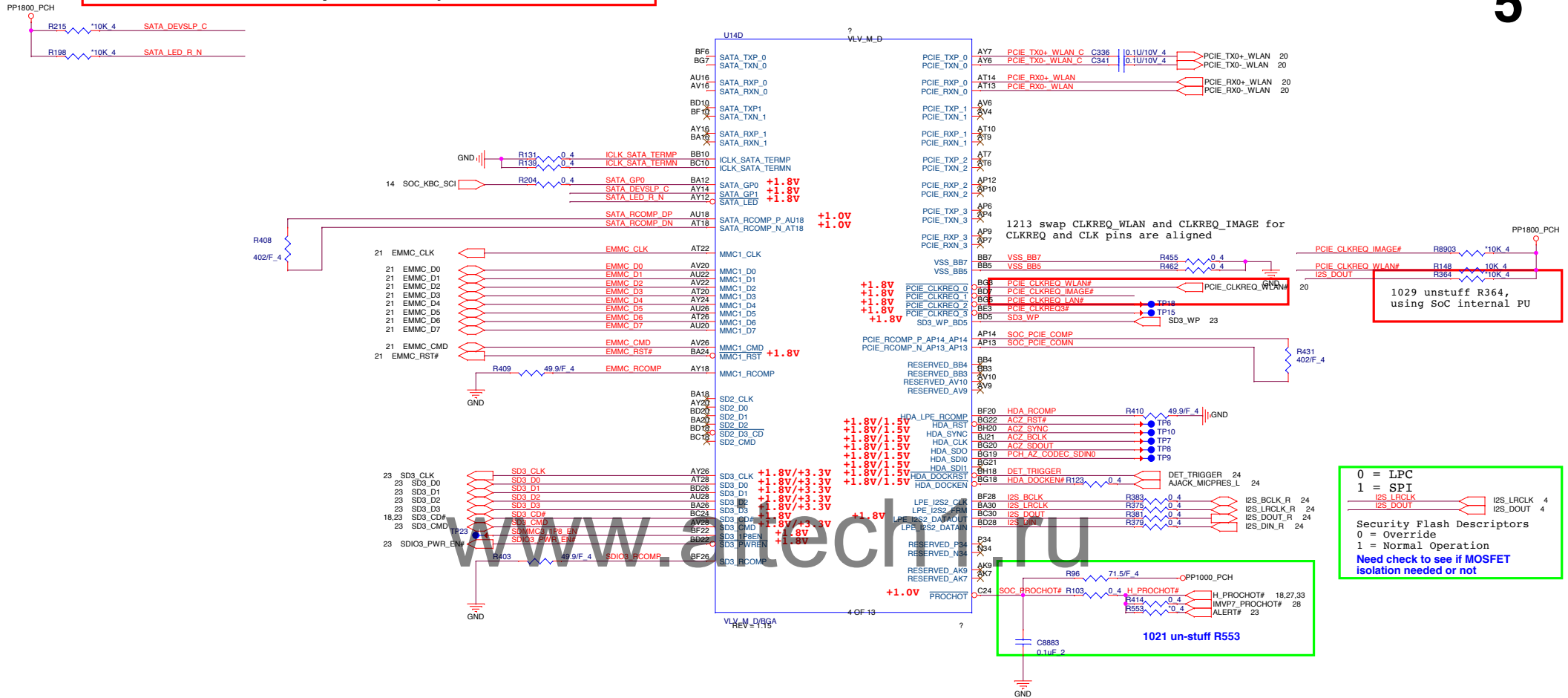
Size
Custom

Document Number
Valley 3/9 (Display)

PROJECT : Peach
Quanta Computer Inc.

Date: Saturday, May 24, 2014 Sheet 4 of 40

1025 Delete complete SSD(connector and caps), unstuff R215
and add test points on SATA signals

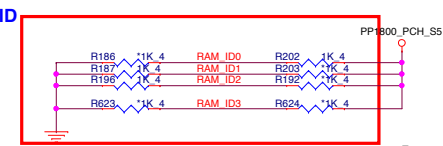


PROJECT : Peach
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Size	Document Number	Rev
Custom	Valley 4/9 (SD/PCIE/SATA)	1A
Date: Saturday, May 24, 2014	Sheet 5 of 40	



RAM ID



Freq. 1600MHz

Vender	RAM_ID	Q PN	Mfr. PN	Channel	Size
Hynix	001	AKD5JGETW11	H5TC4G63AFR-PBA	2CH	4GB
Elpida	000	AKD5JGST410	EDJ4216EFBG-GNL-F	2CH	4GB
Hynix	011	AKD5JGETW14	H5TC4G63AFR-PBR	2CH	4GB
Micron	010	AKD5DGSTL07	MT41K128M16JT-125M:K	2CH	2GB
Elpida	100	AKD5JGST410	EDJ4216EFBG-GNL-F	1CH	2GB
Hynix	101	AKD5JGETW11	H5TC4G63AFR-PBA	1CH	2GB
Hynix	110	AKD5JGETW14	H5TC4G63AFR-PBR	1CH	2GB

C-test sku2

C-test sku4

C-test sku3

C-test sku1

PORT 1 USB CONN
PORT 2 LTE
PORT 3 CCD
PORT 4 BT

MB USB3.0

HUB1

CCD

BT

BT

BT

BT

BT

BT

BT

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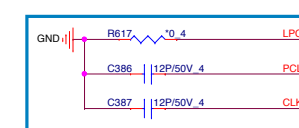
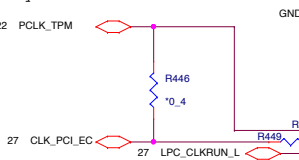
BT

BT

BT

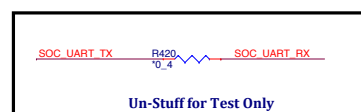
BT

1101 add option BOM R446,R449 for EC CLK for power saving by Intel request

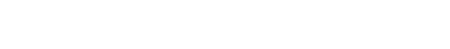
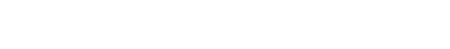
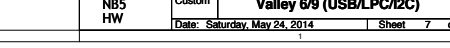
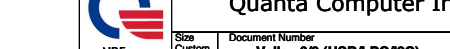
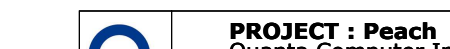
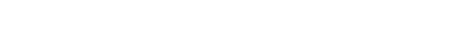
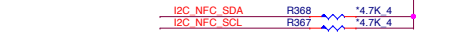
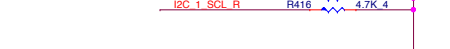
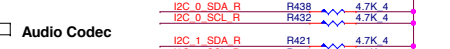


2014_0408_RF suggest

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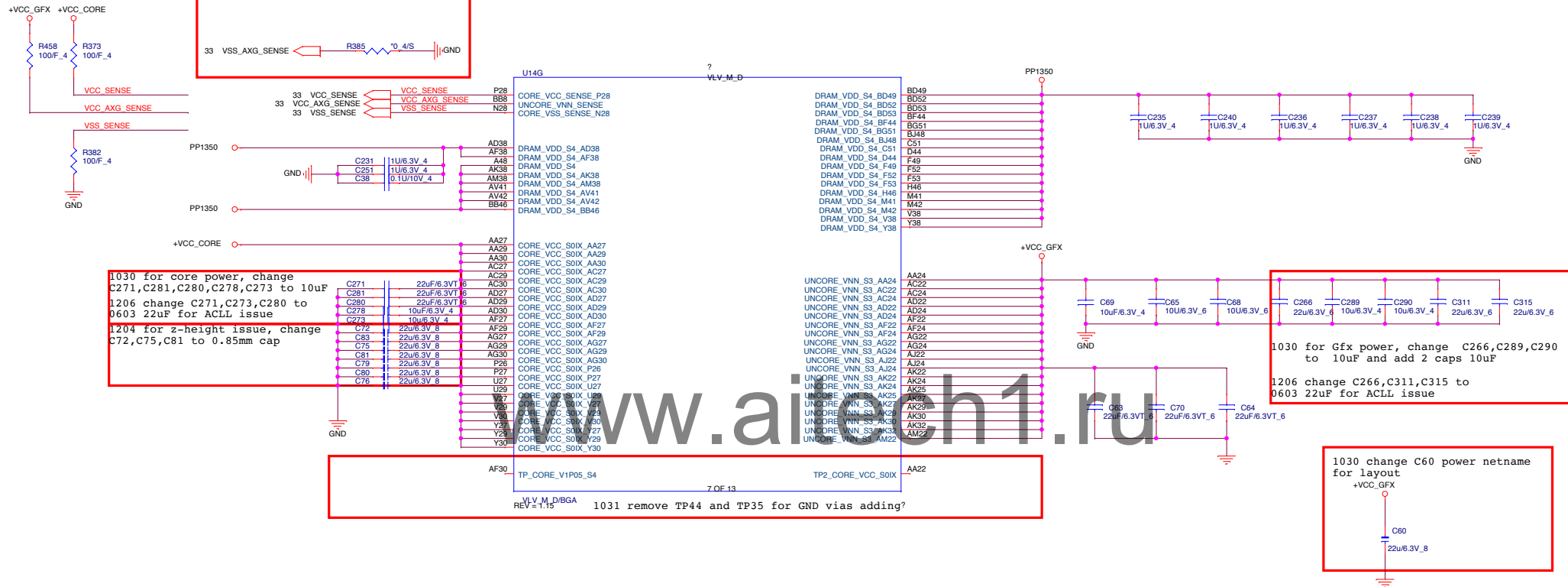
Un-Staff for Test Only

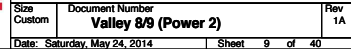


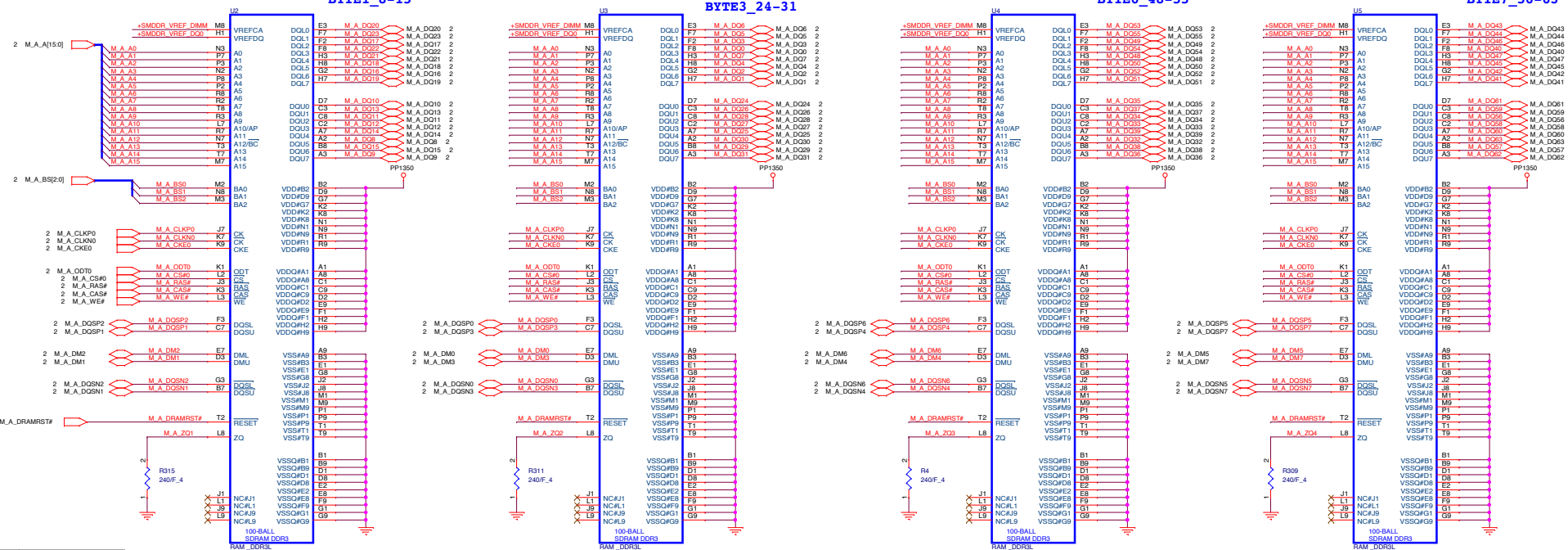
PROJECT : Peach
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 6/9 (USB/LPC/I2C)	1A
Date: Saturday, May 24, 2014	Sheet 7 of 40	

1031 for layout suggestion by intel, VSS_AXG_SENSE didn't connect to VSS_SENSE, will connect the GND via near VCC_AXG_SENSE
1031 for layout, add 0hm between GND and VSS_AXG_SENSE







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Distributed around all DRAM devices (CHA and CHB)

Place these Caps near each X16 Memory Down

1205 add 0.1uFx2 on PP1350 for EMI request

Place these Caps near Memory Down CA & DQ pin

1024 change ODT PU to VTT by Intel request

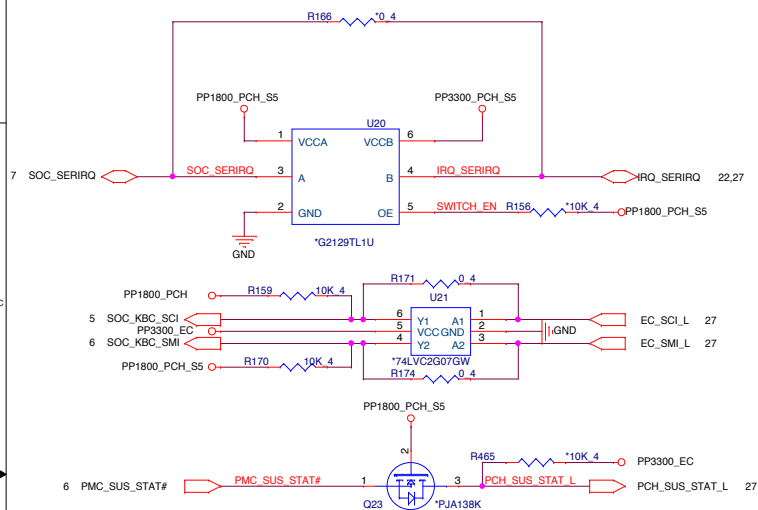
1023 change cap from 0.2pF to 3.3pF

M1 solution

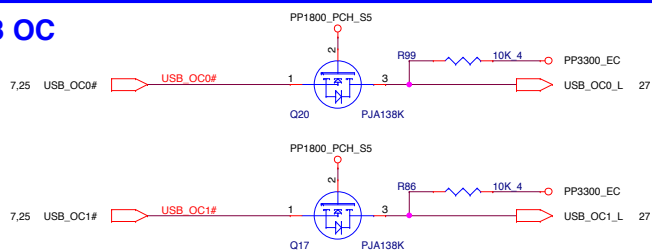
M1 solution

PWRON SEQUENCE

```
9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIRQ of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
```

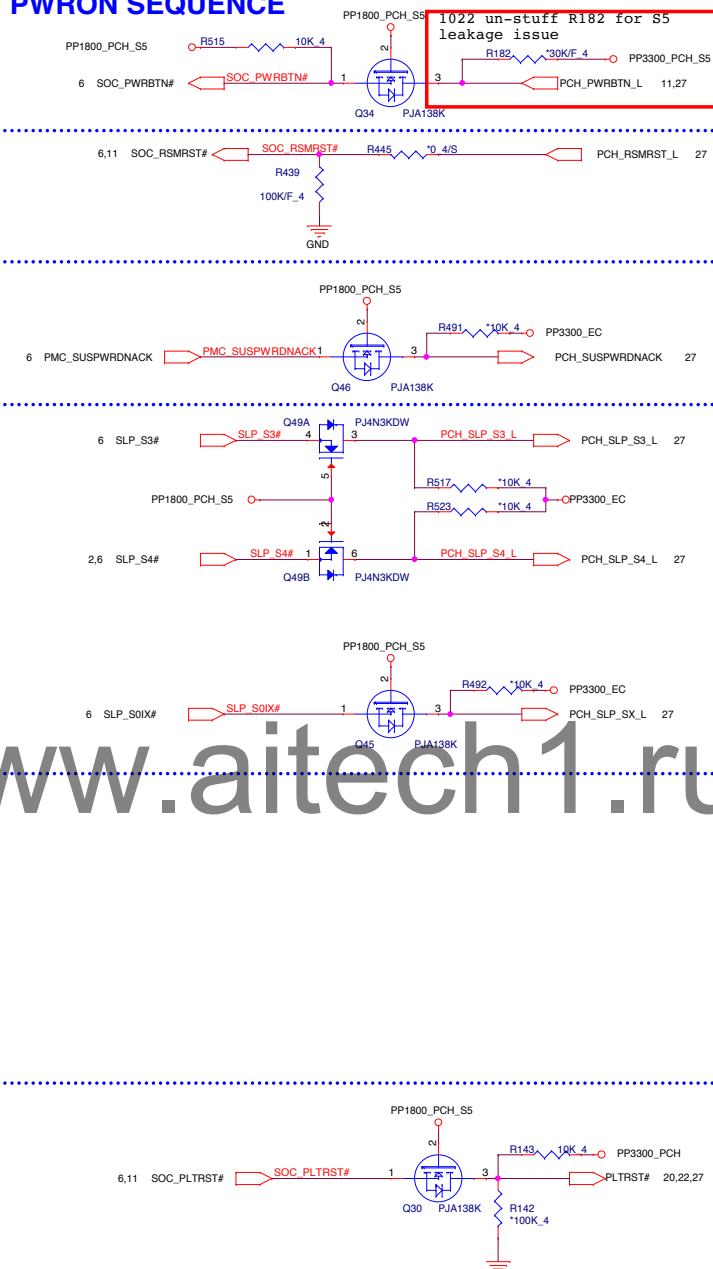


USB OC



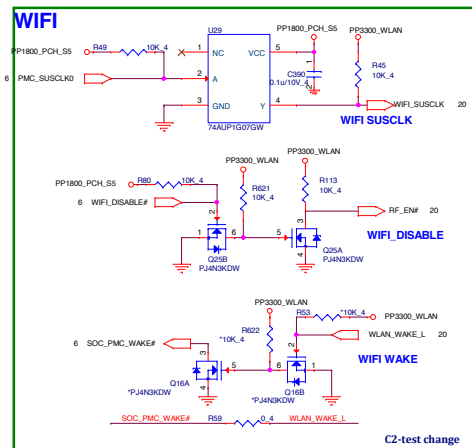
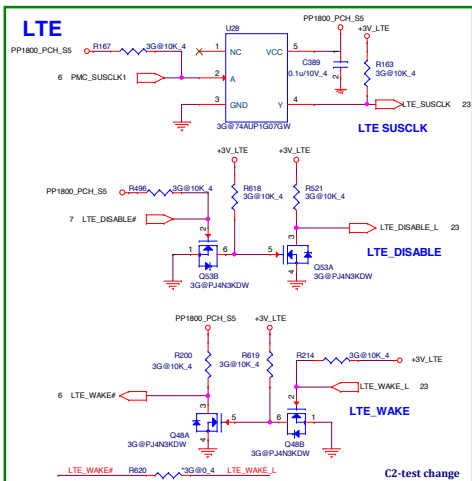
Stuffing for notifying EC

PWRON SEQUENCE

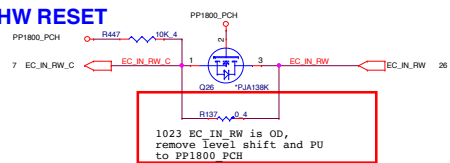


0220 remove SPI_SIO Interface,
Q35,Q36,Q37,Q44,R486,R484,R485,
R483,R426,R429,R427,R428

LTE



HW RESET



Touch Screen(01/27 delete)

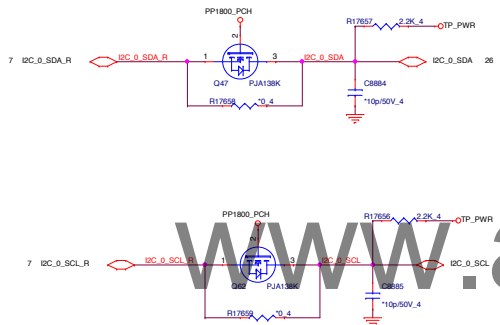
S0

S5

SATA

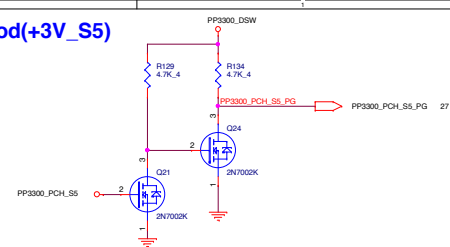
1025 Delete complete SSD(connector and caps)

Track Pad



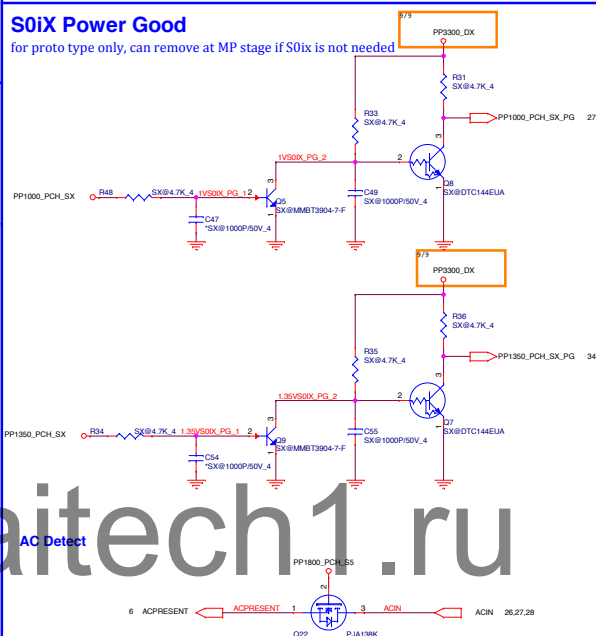
S5 Power Good(+3V_S5)

0830 224

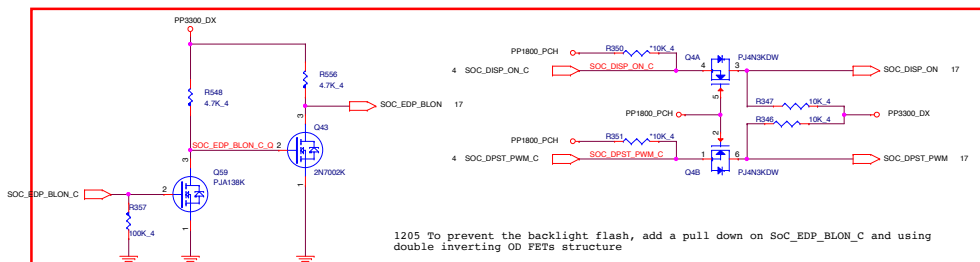


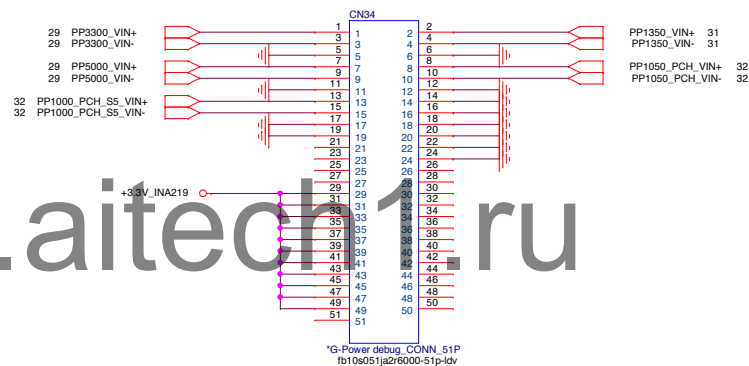
S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed



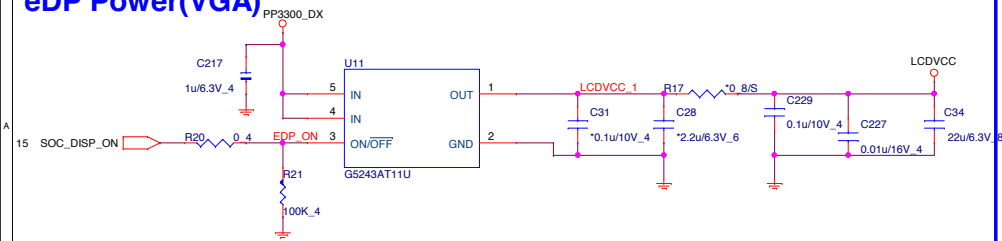
eDP control pin



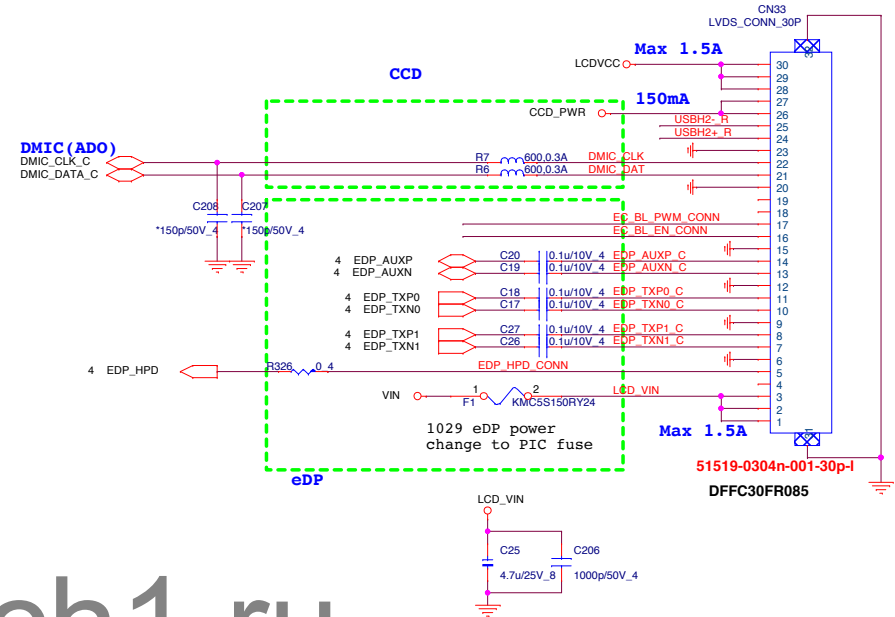


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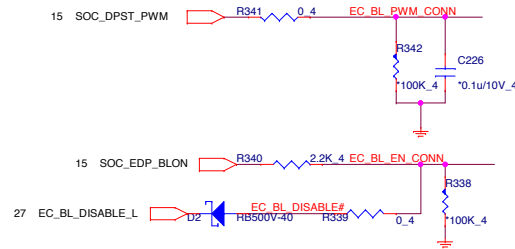
eDP Power(VGA)



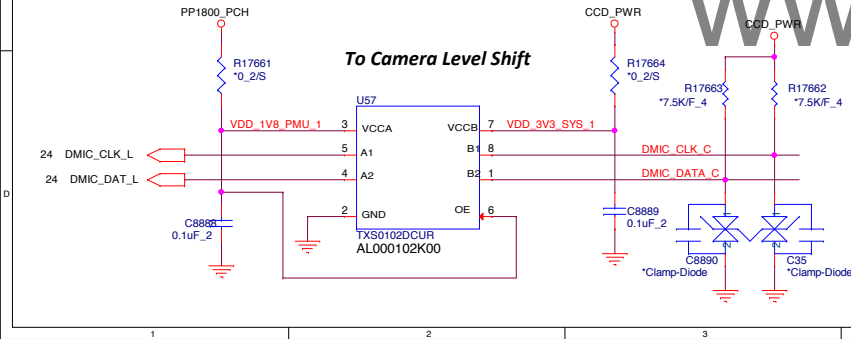
eDP(VGA)



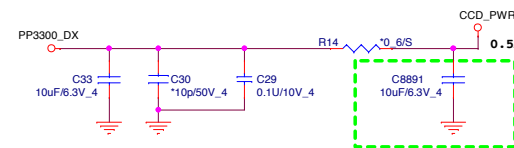
eDP panel control(VGA)



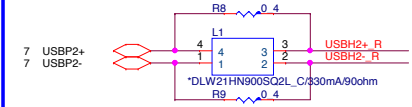
Camera level shift(05/13)



CCD power(CCD)



CCD USB(CCD)



PROJECT : Peach
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Size	Document Number	Rev
Custom	EDP/CCD/DMIC/TS	1A
Date: Saturday, May 24, 2014	Sheet 17 of 40	

GOOGLE Debug Port(MPC)

50 pin BTB is *MUST*, don't use 42 pin

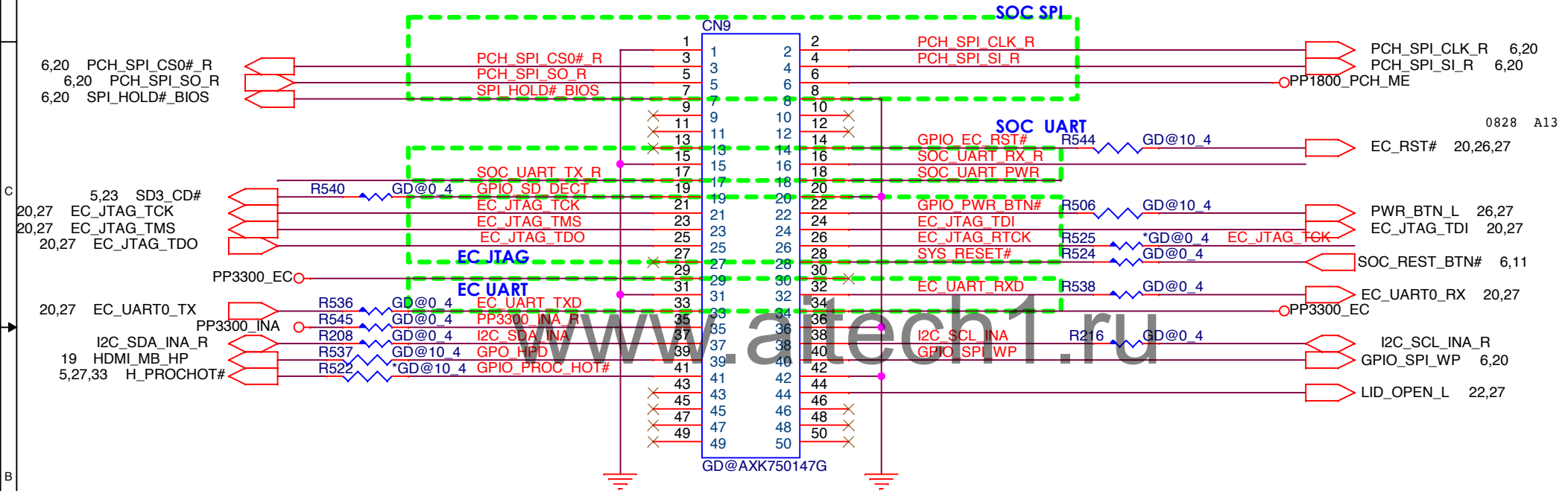
Socket part number AXK750147G

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD

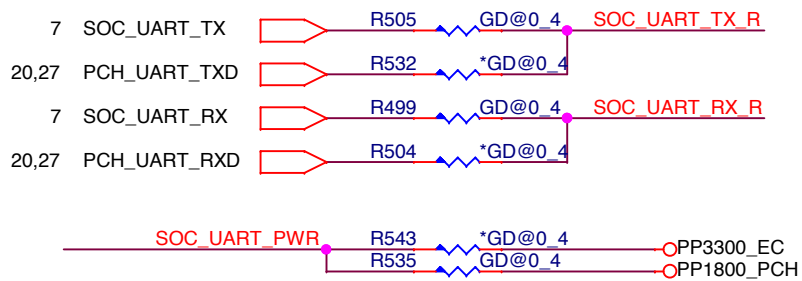
PIN39	OD
PIN41	OD
PIN43	OD
PIN44	OD
PIN45	OD
PIN46	OD
PIN47	OD
PIN48	OD

PIN49 OD
PIN50 OD

18

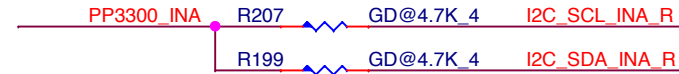


1021 change footprint and PN



9/6 using optional instead of level shifted, default is from SoC

9/13 add pull up



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Size Custom

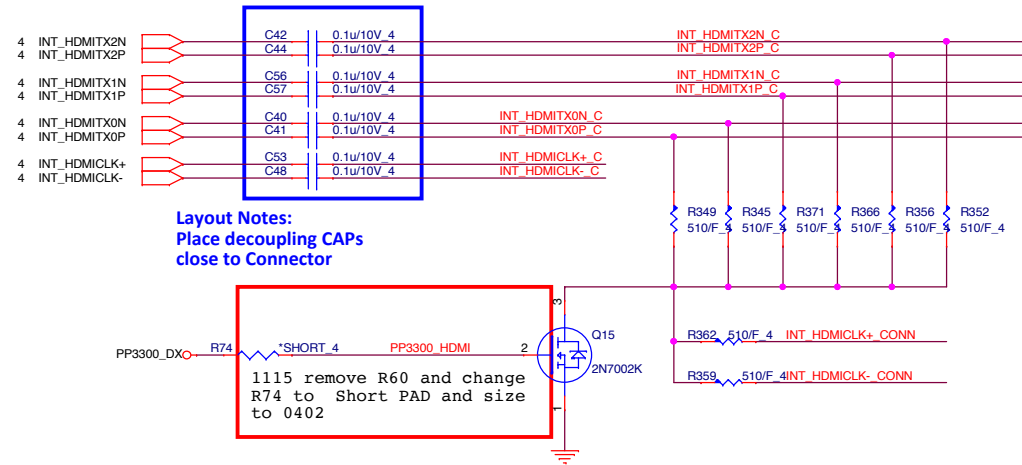
Document Number
Google Debug

Rev
1A

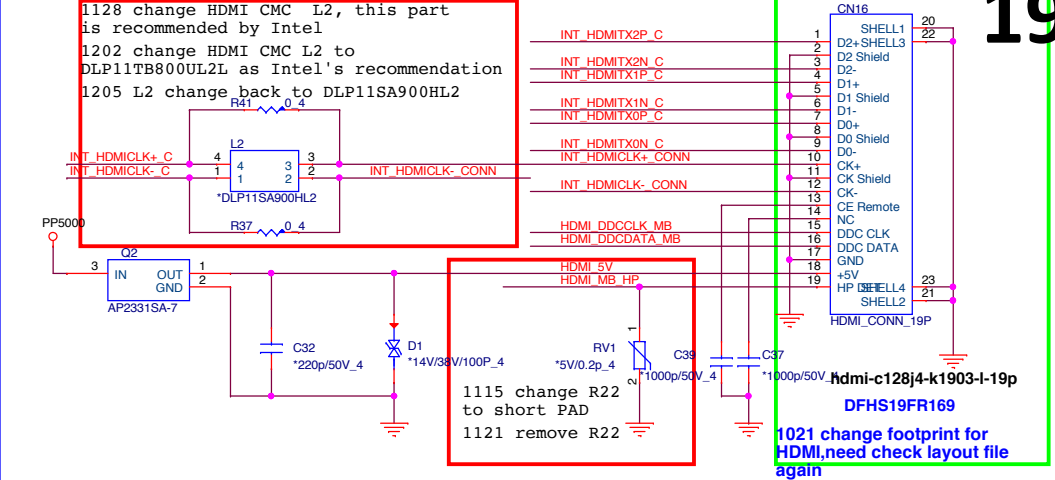
Date: Saturday, May 24, 2014

Sheet 18 of 40

HDMI Cost Reduced level shift (HDM)

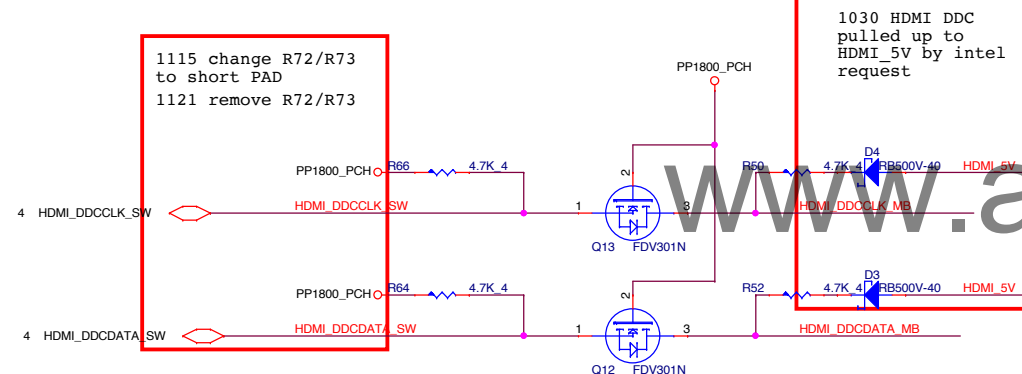


HDMI connector (HDM)

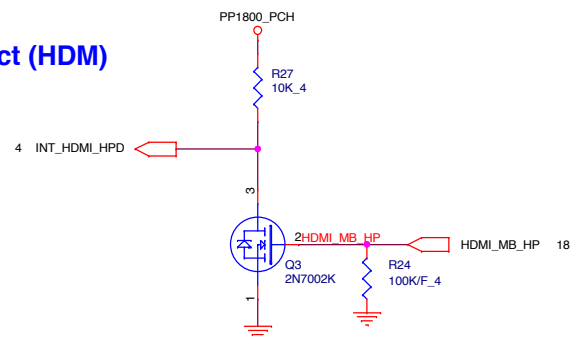


19

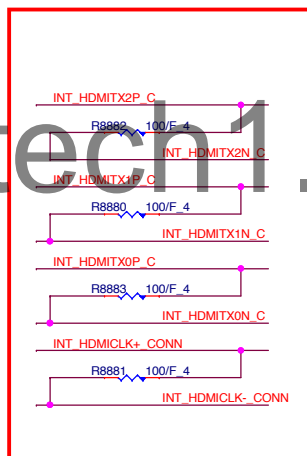
HDMI DDC (HDM)



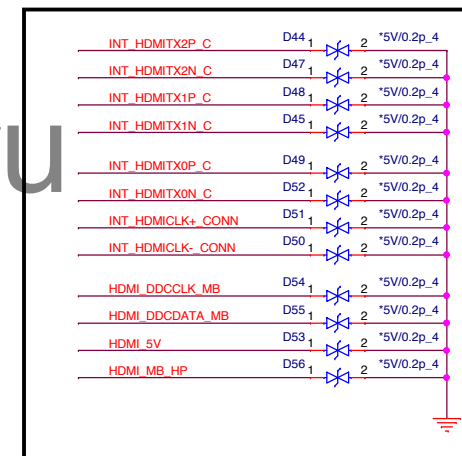
HDMI-detect (HDM)




EMI



ESD 靠近HDMI CONNECTOR(CN16)



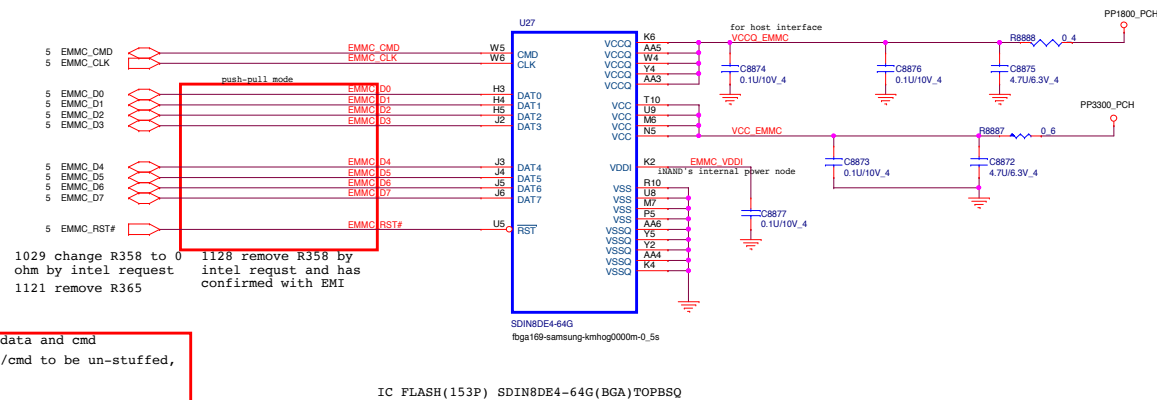


 NB5 HW	PROJECT : Peach Quanta Computer Inc.		
	Size Custom	Document Number WIFI / BT / Image Codec	Rev 1A
Date: Saturday, May 24, 2014	Sheet 20 of 40		

1025 Delete complete SSD(connector and caps)

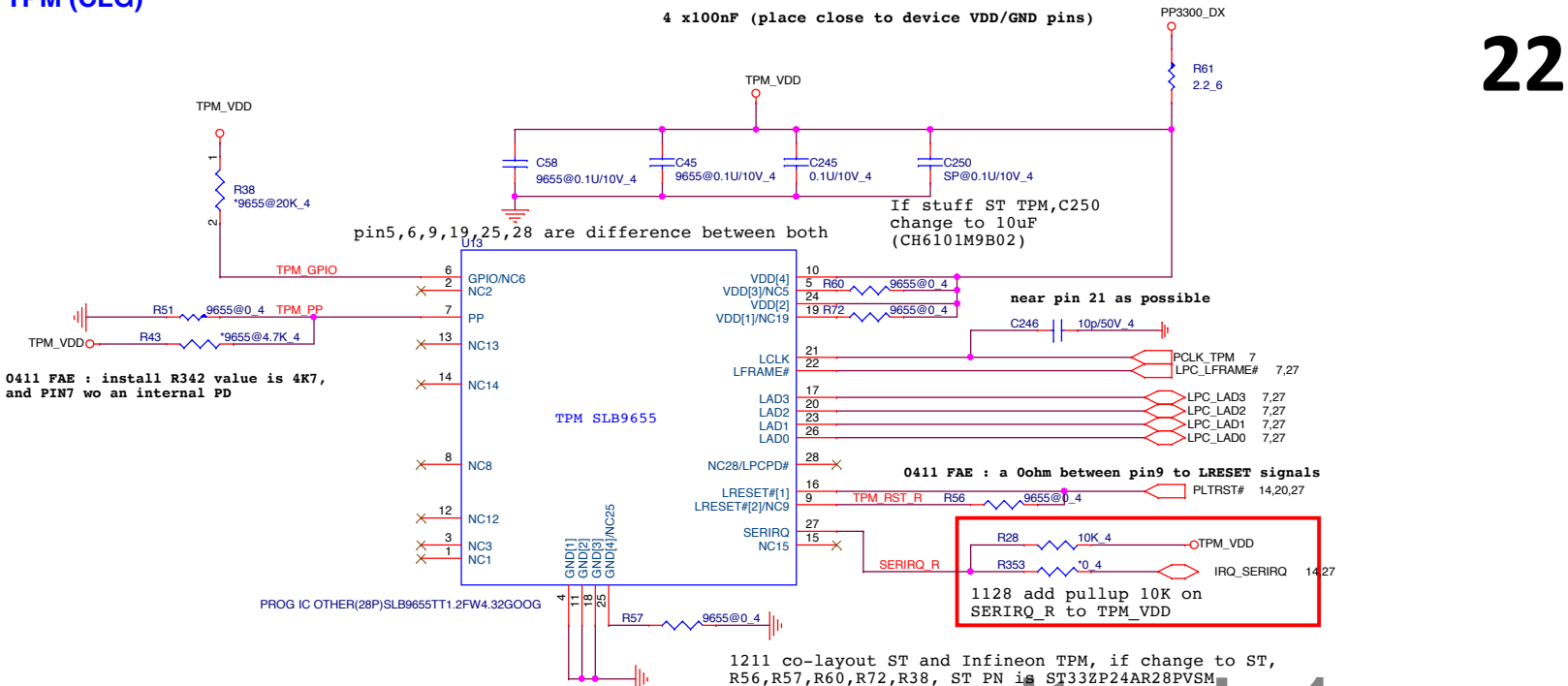
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EMMC (CBS)



1029 remove pulled up resistors for eMMC data and cmd
1211 add back pulled up resistors
1212 all Pulled up resistors of eMMC data/cmd to be un-stuffed, and R361 change to 47K ohm as well

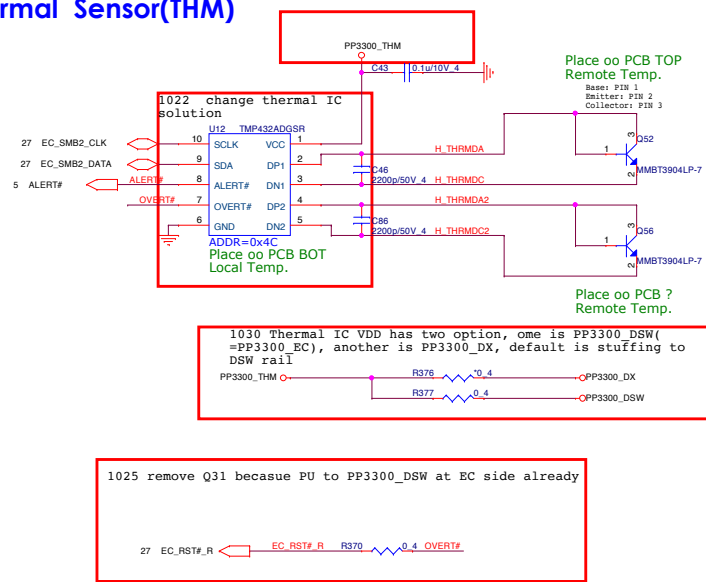
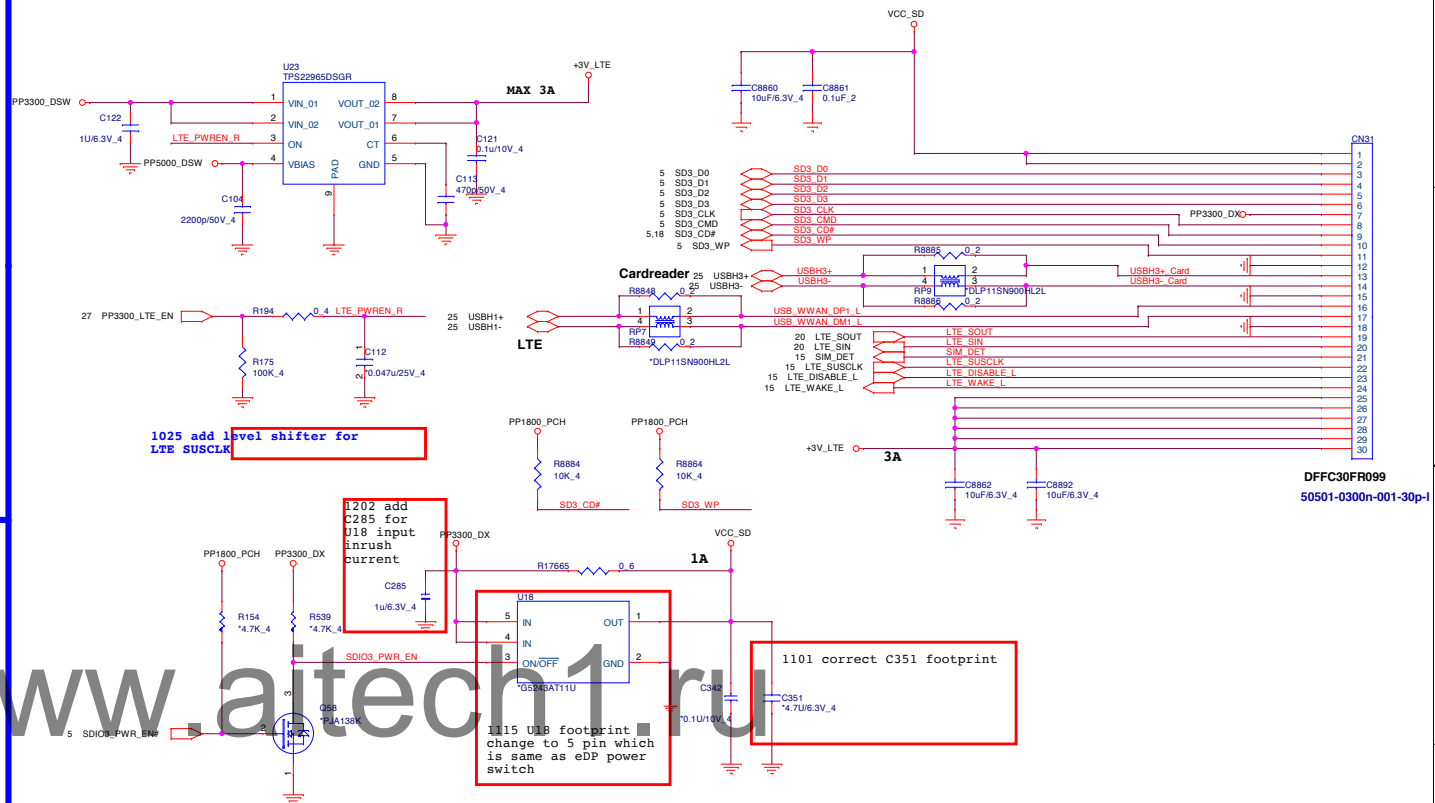
TPM (CLG)



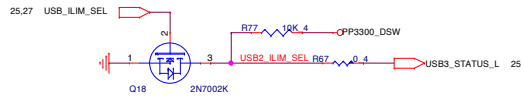
LED(UIF)



Thermal Sensor(THM)

FUNCTION DB
LTE(MNC)

USB Switch Current Control



[illegible]

Normal open

1025 change
headphone footprint
and PN, need check
pin out again

1025 remove pin7

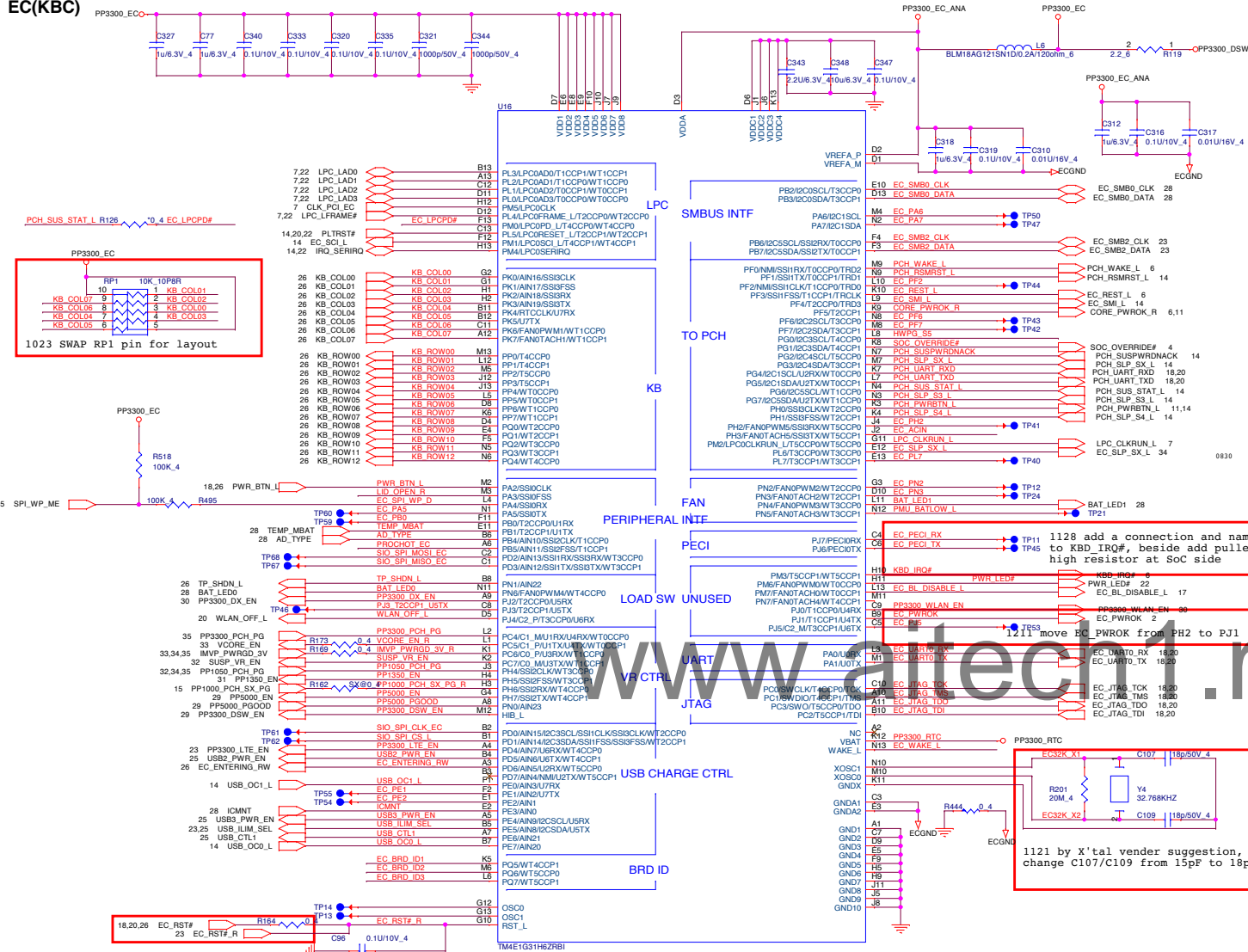
1026 change jack
same as peach1.0

Audio Jack

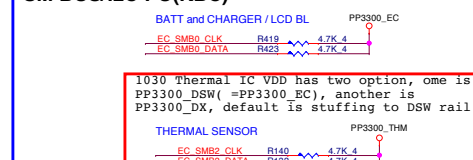
Audio Schematic
after PLUG IN

PIN1 --> MIC
PIN2 --> AGND
PIN3 --> R
PIN4 --> L
PIN5 --> TRANSFER
PIN6 --> HPD

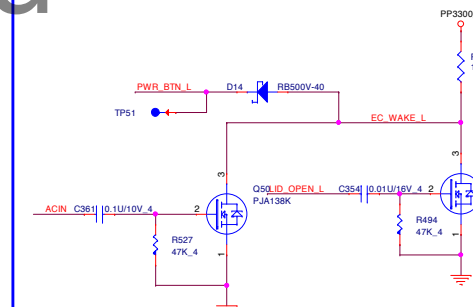
[illegible][illegible]



SM BUS/I2C PU(KBC)



EC HIB WAKE SOURCES



SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

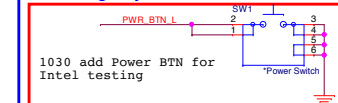
HWPG(KBC)



OD pin list

EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

For testing only



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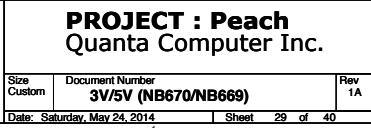
Size Custom Document Number KBC TI TM4E1G31H6ZRB1 Rev 1A
Date: Saturday, May 24, 2014 Sheet 27 of 40

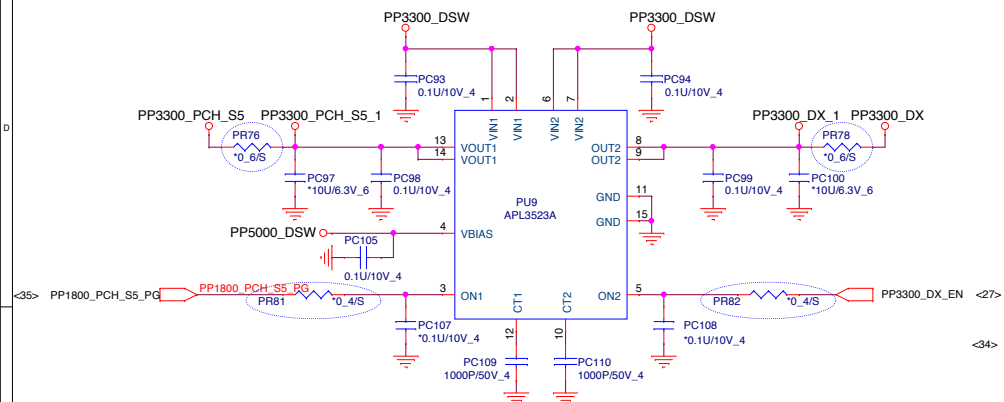


	2-cell	3-cell
PR27	un-stuff	stuff

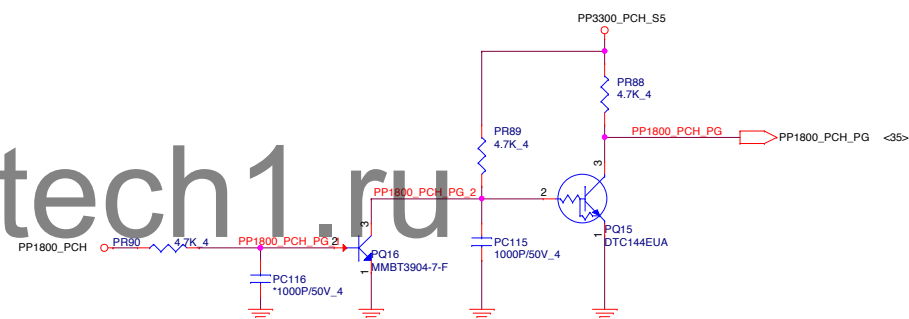
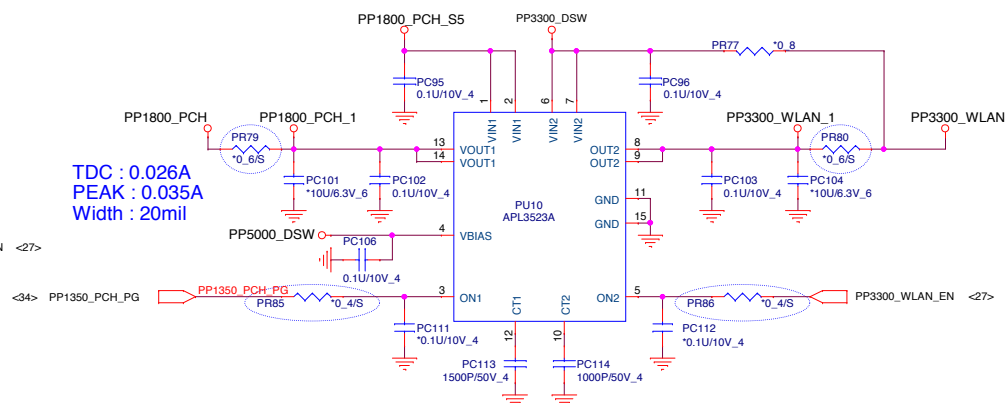


4	3	
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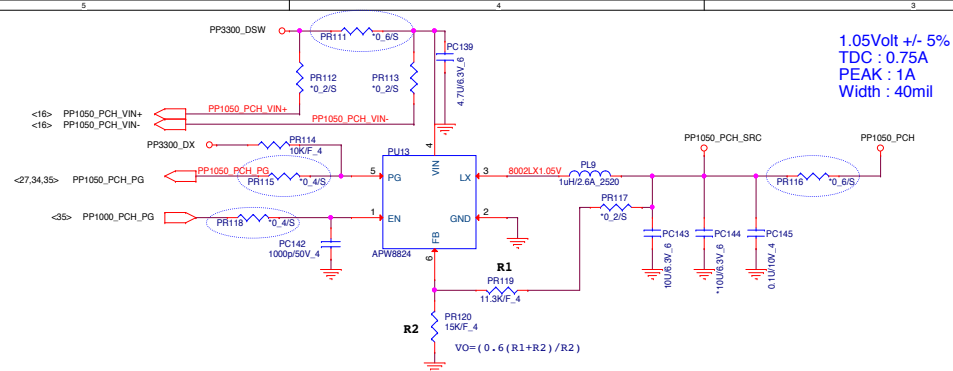
TDC : 0.026A
PEAK : 0.035A
Width : 20mil



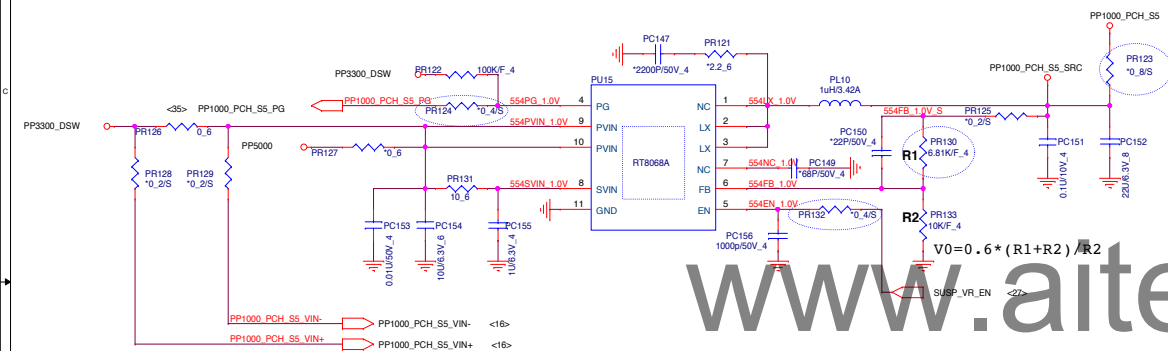
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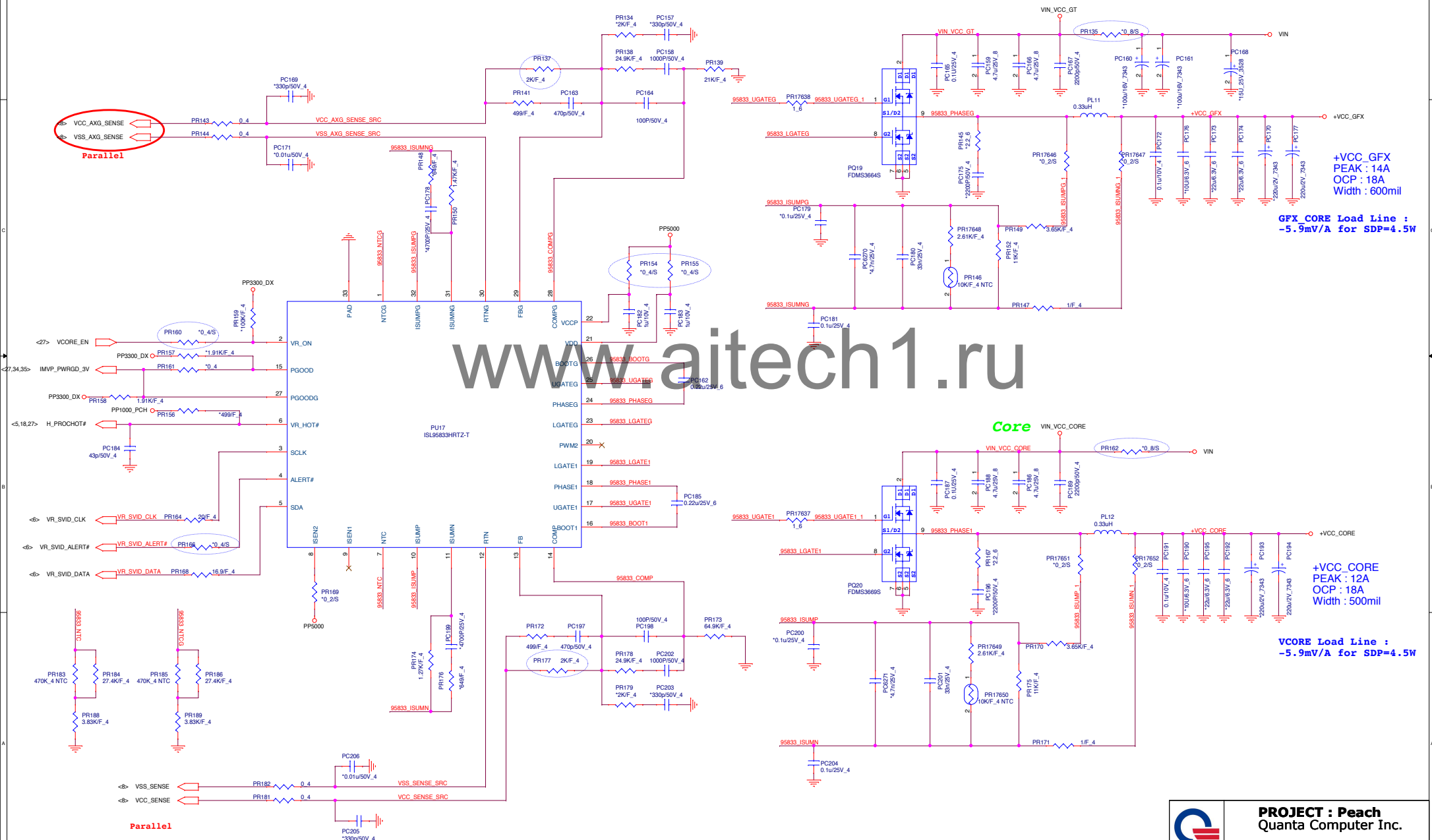
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

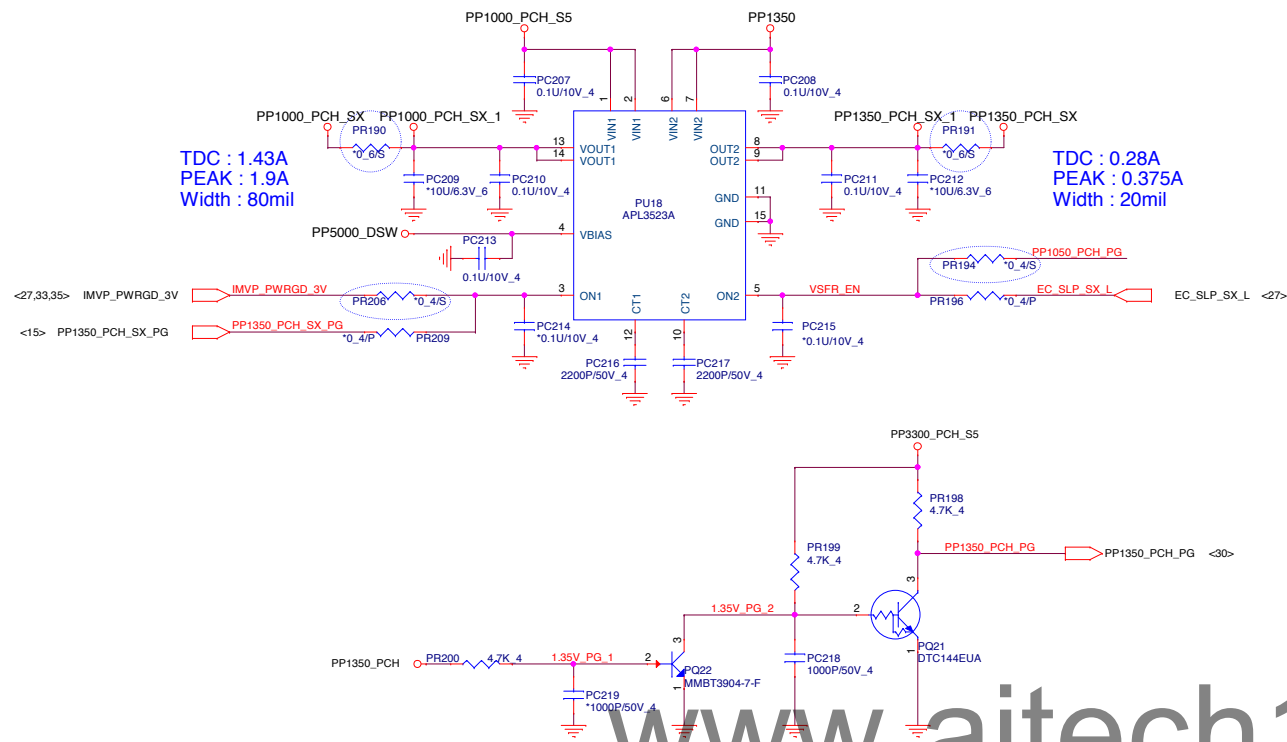


1.0V \pm 5%
TDC : 2.07A
PEAK : 2.75A
Width : 100mil

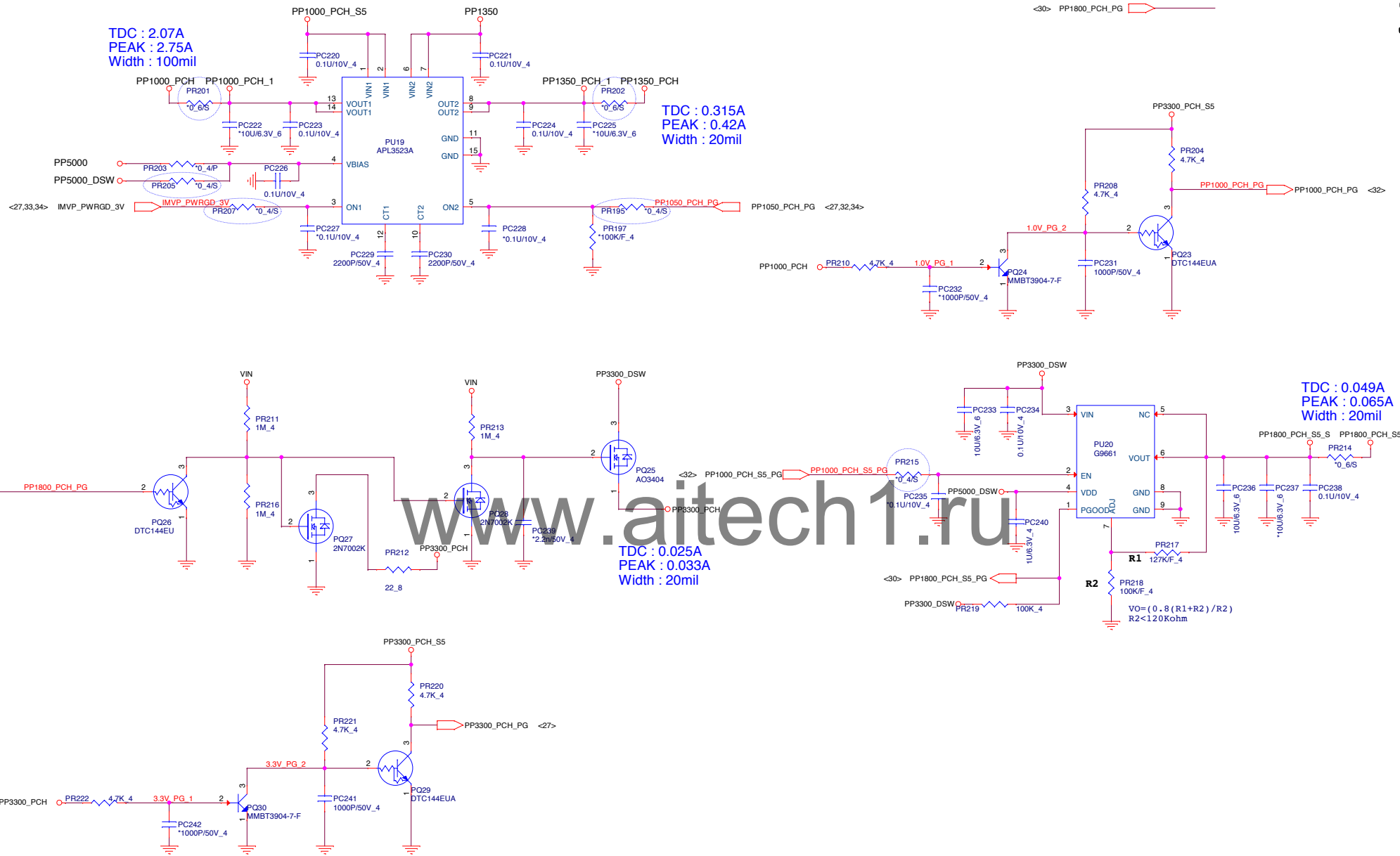


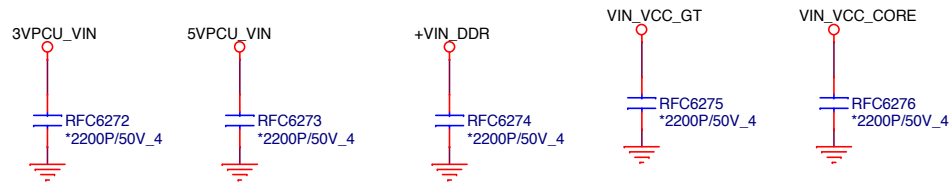
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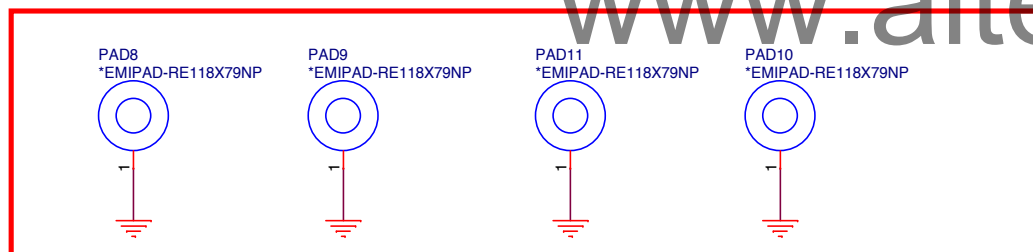




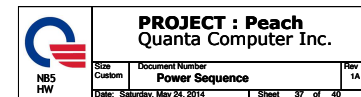
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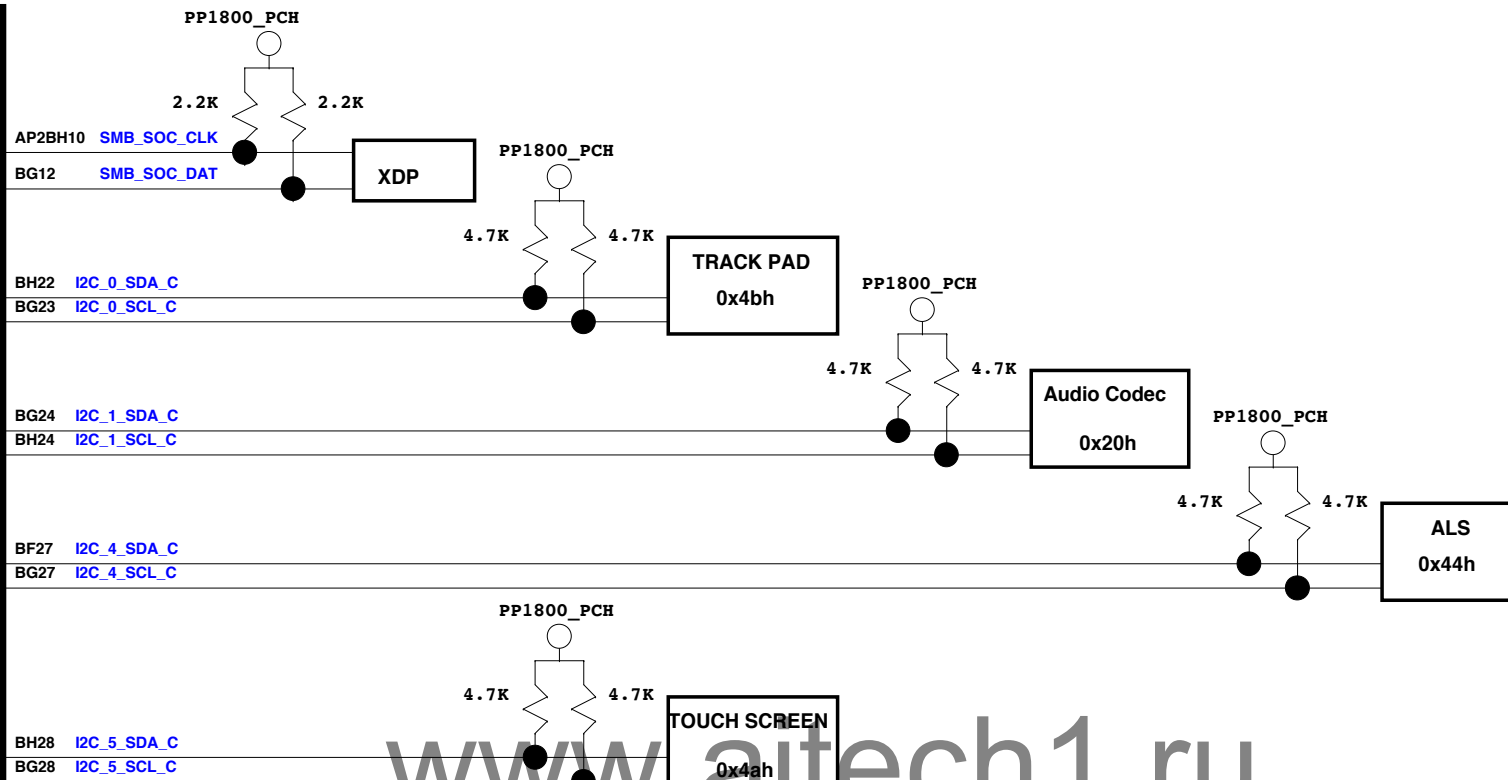


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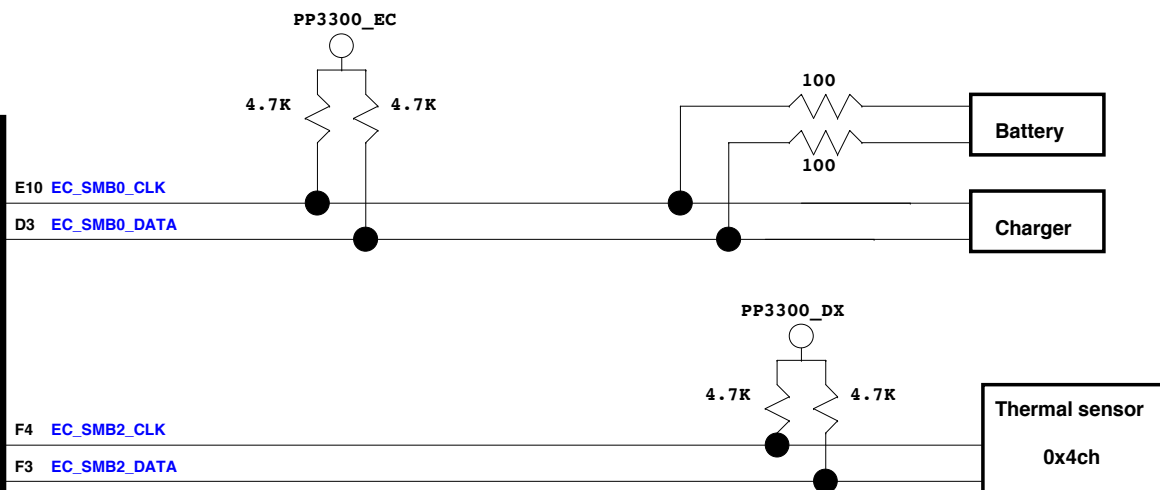


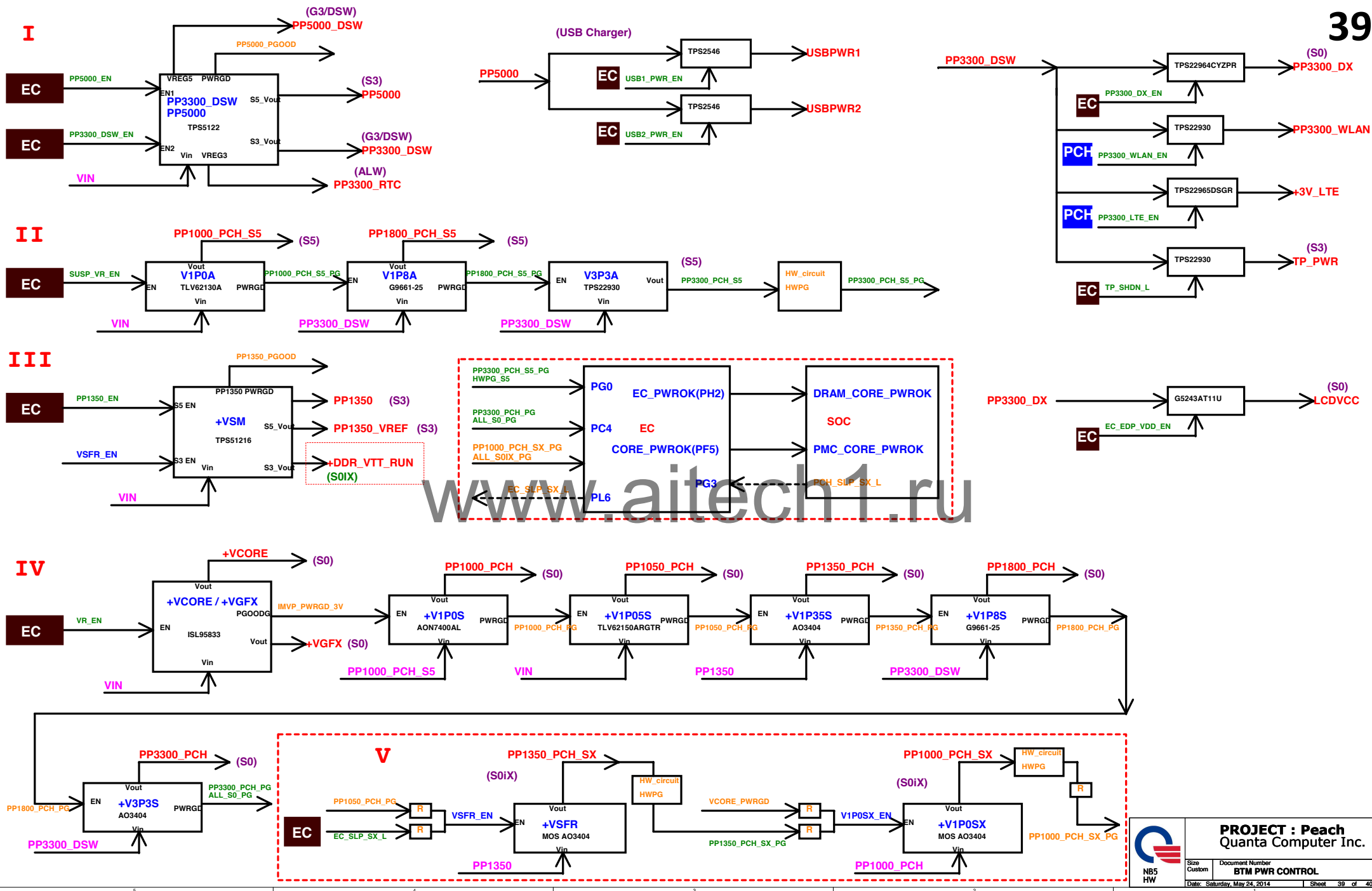
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Size Custom	Document Number BTM PWR CONTROL	Rev 1A
Date: Saturday, May 24, 2014	Sheet 39 of 40	

40